40. (Amended) A semiconductor device comprising a field effect transistor having an interface between a semiconductive silicon layer and a gate oxide layer, structurally characterized by the presence of deuterium at said interface resulting from post-fabrication passivation of said interface in a heated, deuterium gas-enriched atmosphere at a temperature of about 200°C to about 1000°C so as to increase the resilience of the field effect transistor to hot electron effects, said post-fabrication passivation being conducted sufficiently to provide to said transistor a practical lifetime at least about ten times that provided by a corresponding passivation with hydrogen, wherein practical lifetime is taken as 20% transconductance degradation as a result of electrical stress.

48. (Amended) The semiconductor device of claim 40, which comprises a drain formed in said semiconductive silicon layer, a source formed in said semiconductive silicon layer, a channel extending between the drain and the source, said gate oxide layer over said channel, said interface between said gate oxide layer and said channel, and conductive contacts for said drain, said source and said gate oxide; and

wherein said post-fabrication passivation [provides] is carried out after formation of said conductive contacts and produces a structure including covalently-bound deuterium populating said interface.

Please add the following new claims 62-65:

62. (New) A semiconductor device comprising a field effect transistor having an interface between a semiconductive silicon layer and a gate oxide layer, a drain formed in said semiconductive silicon layer, a source formed in said semiconductive silicon layer, a channel extending between the drain and the source, said gate oxide layer over said channel, said interface between said gate oxide layer and said channel, and conductive contacts for said drain, said source and said gate oxide; said semiconductive device structurally characterized by post-fabrication heating of the device after formation of said contacts, in a deuterium gas-enriched atmosphere at a temperature of about 200°C to about 1000°C to provide deuterium at and to passivate said interface so as to increase the resilience of the field effect transistor to hot electron effects.

63. (New) The semiconductor device of claim 62 wherein said gate oxide layer comprises silicon dioxide.

64. (New) The semiconductor device of claim 62, wherein said semiconductive silicon layer is a crystalline silicon layer.

65. (New) The semiconductor device of claim 62, comprising deuterium atoms from said post-fabrication passivation covalently bonded at said interface.